UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/553,580	06/05/2006	Michinobu Tanioka	19246	1492

23389 7590 12/11/2007

SCULLY SCOTT MURPHY & PRESSER, PC
400 GARDEN CITY PLAZA
SUITE 300
GARDEN CITY, NY 11530

EXAMINER	
VELEZ, ROBERTO	

ART UNIT	PAPER NUMBER
2829	

MAIL DATE	DELIVERY MODE
12/11/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/553,580	TANIOKA ET AL.	
	Examiner	Art Unit	
	Roberto Velez	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☒ Claim(s) *11-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 10/26/2007 have been fully considered but they are not persuasive.

2. Applicant argues that Esashi does not disclose wiring layers mounted on the base member as recited by claim 1. The Examiner respectfully disagrees. As stated in the last Office Action, Esashi shows (Fig. 1) the wiring layers 12 mounted on the base member 11. The claim does not particularly and uniquely defines the term "mounted" so as to distinguish it from the applied prior art. During patent examination, the claims are given their broadest reasonable interpretation. See MPEP 2111. The claimed "wiring layers mounted on the base member" is broadly claimed; therefore, broadly interpreted. The wiring layers 12 of Esashi are "buried" on the through hole 11D of base member 11 as shown in Figures 8G-8H. The through holes 11D are formed in inner walls of base member 11. The wiring layers 12 are "mounted" to these inner walls of the base member 11 at the moment that the wiring layers 12 are "buried" on the through holes 11D. In this manner, the wiring layers 12 are mounted to the base member 11. Also, the wiring layers of Esashi are elements affixed to the base member, thus, clearly and fairly considered "mounted on the base" as claimed. Specifically applied to Applicant's arguments, the base member is an element to which the wiring layers are affixed (see Fig. 1); thus, clearly and fairly characterized as wiring layers mounted on the base. The wiring layers are fixed to the base member, thus, the wiring layers are mounted on the base member.

3. In addition, Applicant argues that Esashi does not disclose wherein the first metal layers and the second metal layers are separated from each other. The Examiner respectfully disagrees. As stated in the last Office Action, Esashi shows (Fig. 1) wherein the first metal layers 14 and the second metal layers 13C are separated from each other. The claim does not particularly and uniquely defines the term "separated" so as to distinguish it from the applied prior art. During patent examination, the claims are given their broadest reasonable interpretation. See MPEP 2111. The claimed "first metal layers and the second metal layers are separated from each other" is broadly claimed; therefore, broadly interpreted. Esashi shows (Fig. 1) beam member 13 divided into parts or step-portions, i.e., portions 13C, 13D and 13E; thus, beam 13 is "separated" into portions 13C, 13D and 13E. Further, it is clearly shown (Fig. 1) that first metal layer 14 is formed on tip portion 13E spaced apart from portion 13C by coupling portion 13D; thus, separated from portion 13C referred to as second metal layer. Also, Esashi discloses that beam 13 is formed in level differences (Col. 5, Ln 37-39). Therefore, portions 13C, 13D and 13E are "separated" in different levels.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-2 and 4-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Esashi et al. (US Pat. 6,747,465).

Regarding claim 1, Esashi et al. shows (Figures 1-12) an inspection probe for inspecting electrical properties of a semiconductor device, comprising: a base member [11]; wiring layers [12] mounted on the base member [11]; probe pins [15] having tips [13E], electrically connected to the wiring layers [12], protruding from the base member [11]; first metal layers [14] provided to tips [13E] of the probe pins [15]; and second metal layers [13C] formed on the wiring layers [12], wherein the first metal layers [14] and the second metal layers [13C] are separated from each other.

Regarding claim 2, Esashi et al. discloses everything as claimed above in claim 1; in addition, Esashi et al. discloses wherein the first metal layers [14] are made of a material having good contact properties selected depending on a material of external terminal electrodes [P] of the semiconductor device [W] (Col. 10, Ln 9-32).

Regarding claim 4, Esashi et al. discloses everything as claimed above in claim 1; in addition, Esashi et al. shows (Fig. 1) wherein the base member [11] has a plurality of the probe pins [15].

Regarding claim 5, Esashi et al. discloses everything as claimed above in claim 1; in addition, Esashi et al. discloses wherein the first metal layers [14] and the second metal layers [13C] are made of the homogeneous material (titanium as disclosed in Col. 5, Ln 23-32).

Regarding claim 6, Esashi et al. discloses everything as claimed above in claim 1; in addition, Esashi et al. discloses wherein the first metal layers [14] and the second

metal layers [13C] are made of the heterogeneous material (gold and titanium as disclosed in Col. 5, Ln 23-32).

Regarding claim 7, Esashi et al. discloses everything as claimed above in claim 1; in addition, Esashi et al. discloses wherein the first metal layers [14] have hardness higher than that of the external terminal electrodes [P] of the semiconductor device [W] (Col. 5, Ln 28-32).

Regarding claim 8, Esashi et al. discloses everything as claimed above in claim 1; in addition, Esashi et al. shows (Fig. 6A) wherein a region [13E] for forming each first metal layer [14] has a width wider than or equal to half of the width of the probe pins [15] and a length longer than or equal to the sum of 1.0 time the size of the electrodes [P], **the distance that the inspection probe is moved after the inspection probe coming in contact with the electrodes, the longitudinal positional tolerance of the probe pins, and the length determined based on the positional tolerance of the electrodes.*

**This claim language is not given weight because claim 8 is claiming an apparatus, not a process of using the apparatus.*

Regarding claim 9, Esashi et al. discloses everything as claimed above in claim 1; in addition, Esashi et al. shows (Fig. 3) wherein the probe pins [15] form an angle of 0 to 45 degrees with respect to a face on which the electrodes [P] of the semiconductor device [W] are formed.

Regarding claim 10, Esashi et al. discloses everything as claimed above in claim 1; in addition, Esashi et al. shows (Figures 1-2) a flexible, electrically connectable wiring substrate [16] placed between the base member [11] and a inspection substrate [21]

and a backup plate [24], mounted on the inspection substrate [21], for mounting the base member [11] thereon if the electrodes [P] of the semiconductor device [W] are arranged at sides thereof, correspond to multiple pins [15], and must be connected to the inspection substrate [21] (Col. 6, Ln 28-39).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Esashi et al. (US Pat. 6,747,465).

Regarding claim 3, Esashi et al. discloses everything as claimed above in claim 1.

Esashi et al. is silent about disclosing wherein the second metal layers have a volume resistivity less than that of the wiring layers.

It would have been obvious to have second metal layers with a volume resistivity less than that of the wiring layers for the purpose of controlling the amount of current or voltage being applied to the electrodes in order to avoid damaging the electrodes.

Allowable Subject Matter

8. Claims 11-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject manner: the prior art of record, taken alone or in combination, fails to disclose or render obvious, an inspection probe comprising a support substrate which is integrated with peripheral portions of the base member with an adhesive member placed there between and which is made of the same material as a material of the base member, said support substrate being mounted on the inspection substrate, wherein the backup plate has a protrusive portion at a center area thereof such that the probe pins form a predetermined angle with respect to the electrodes of the semiconductor device, as further disclosed in claim 11.

Claims 12-20 depending from claim 11 are also objected for the same reason.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

11. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Roberto Velez whose telephone number is 571-272-8597. The examiner can normally be reached on Monday-Friday 8:00am- 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on 571-272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

RV

Roberto Velez
Patent Examiner

HA TRAN NGUYEN
SUPERVISORY PATENT EXAMINER

12/10/7